

Fig. 1

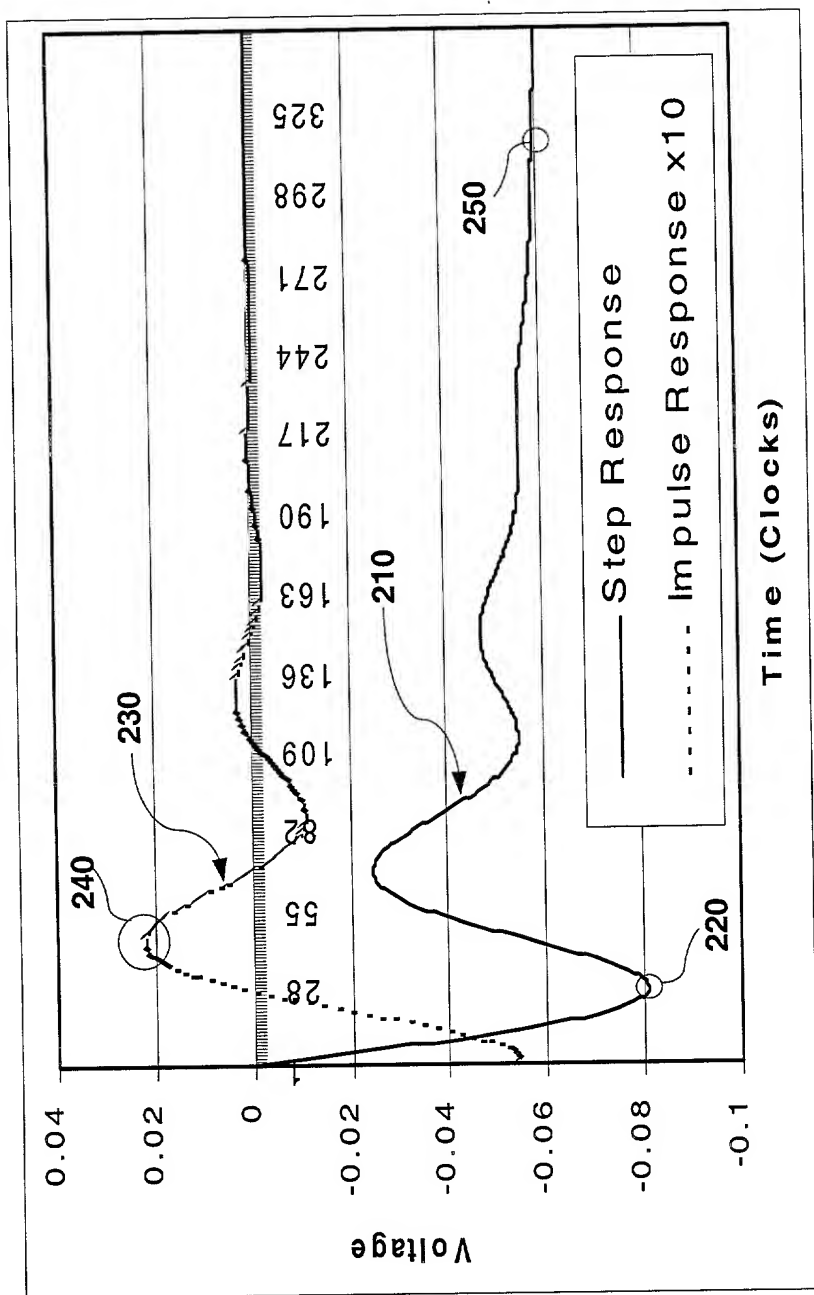


Fig. 2

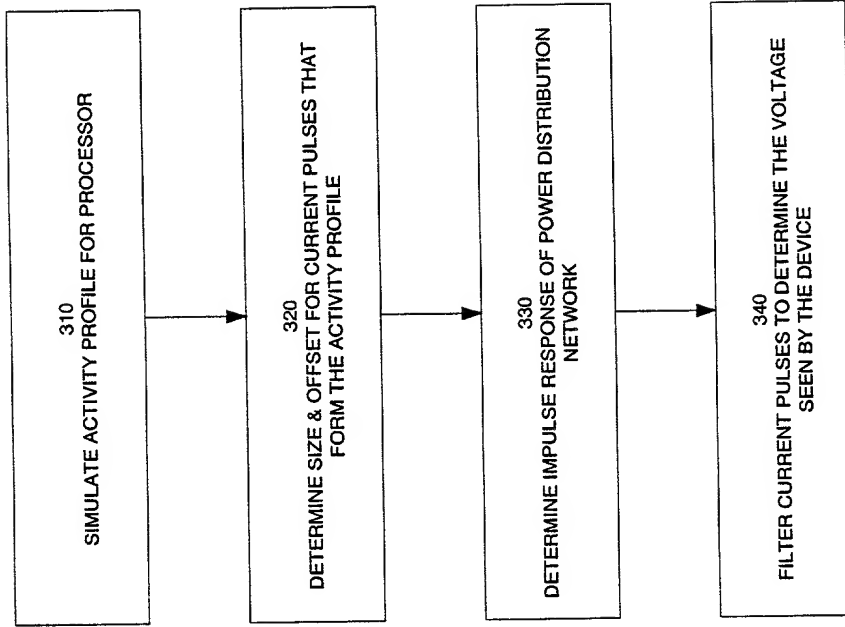


Fig. 3

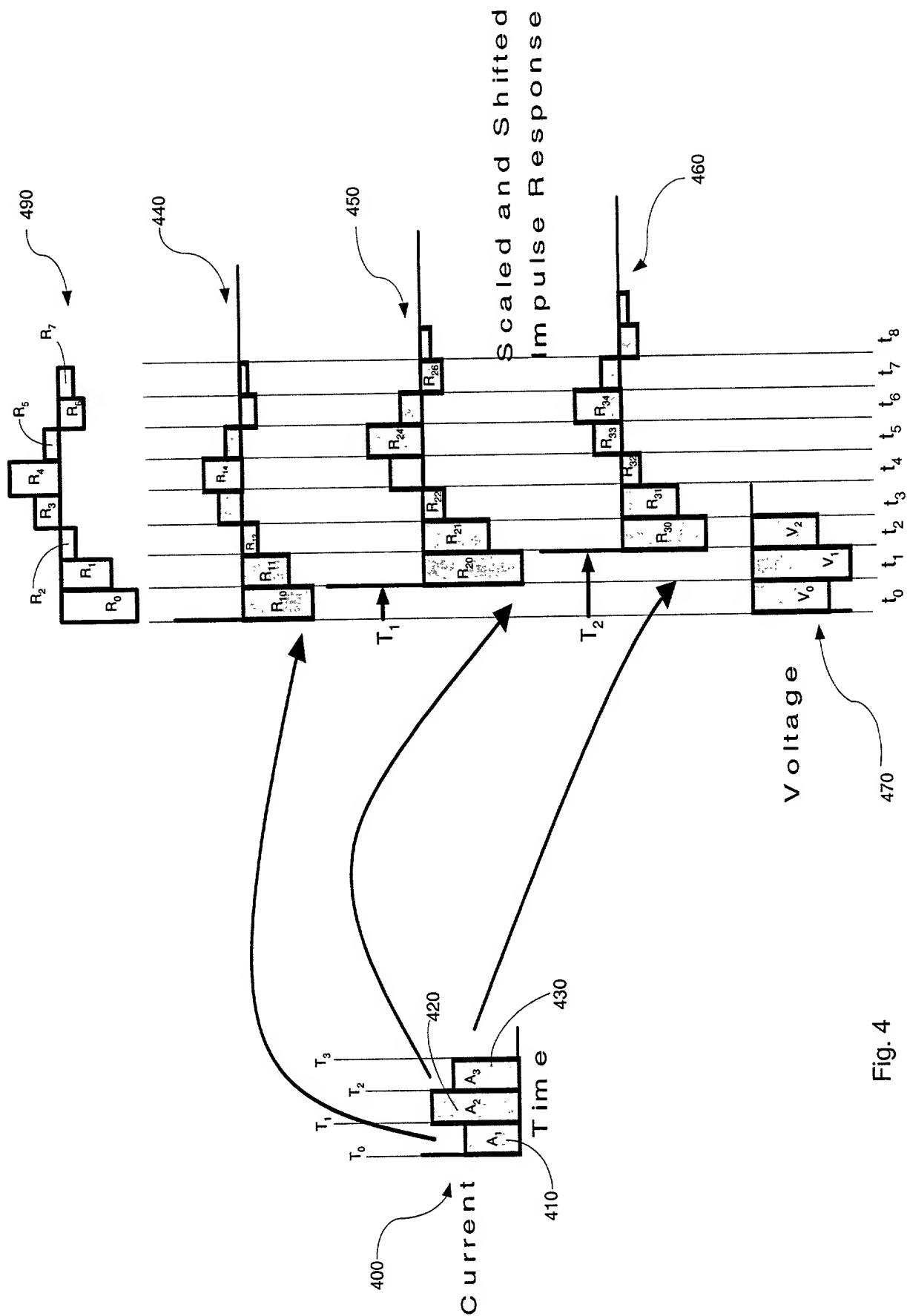


Fig. 4

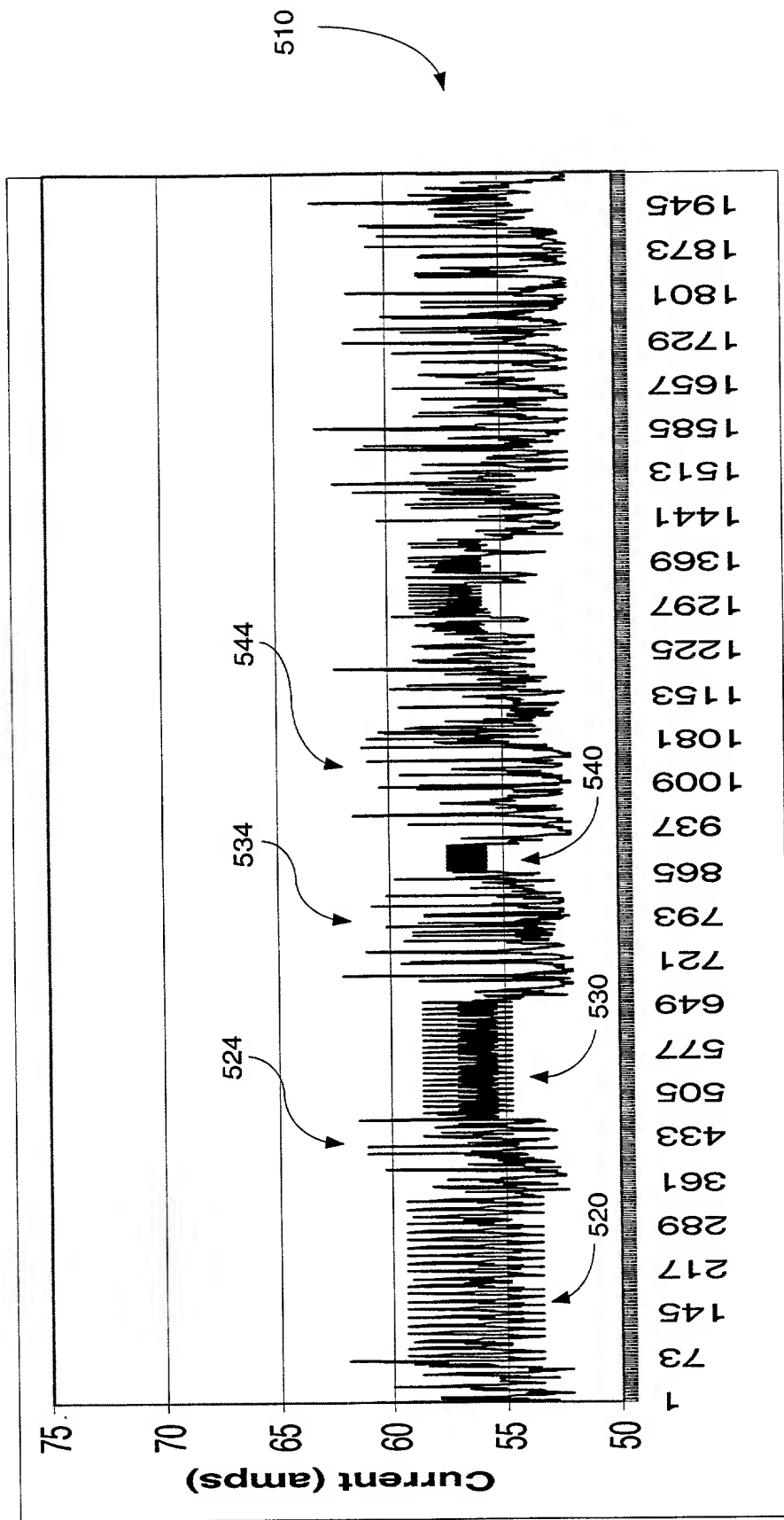


Fig. 5

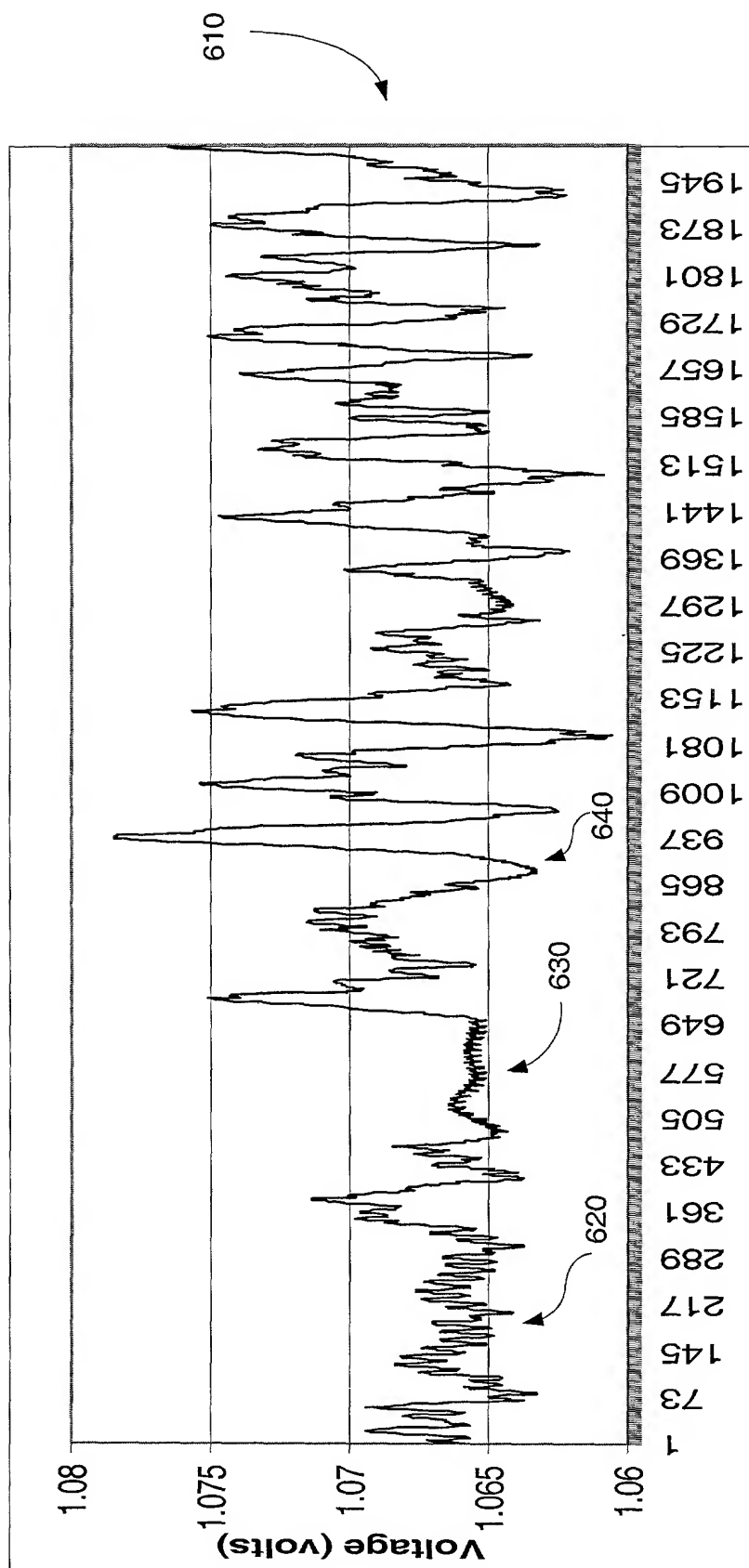


Fig. 6

FIG. 7 is a block diagram of a system 700 in accordance with one embodiment of the present invention. The system 700 includes a processor 710, a power supply 780, a system logic 770, a main memory 740, a non-volatile memory 750, and a peripheral device(s) 760. The processor 710 is connected to the power supply 780 and the system logic 770. The system logic 770 is connected to the main memory 740, the non-volatile memory 750, and the peripheral device(s) 760. The processor 710 also includes a cache 720 and a bus 730. The cache 720 is connected to the bus 730, which is connected to the system logic 770. The cache 720 includes a first set of cache lines 724 and a second set of cache lines 724'.

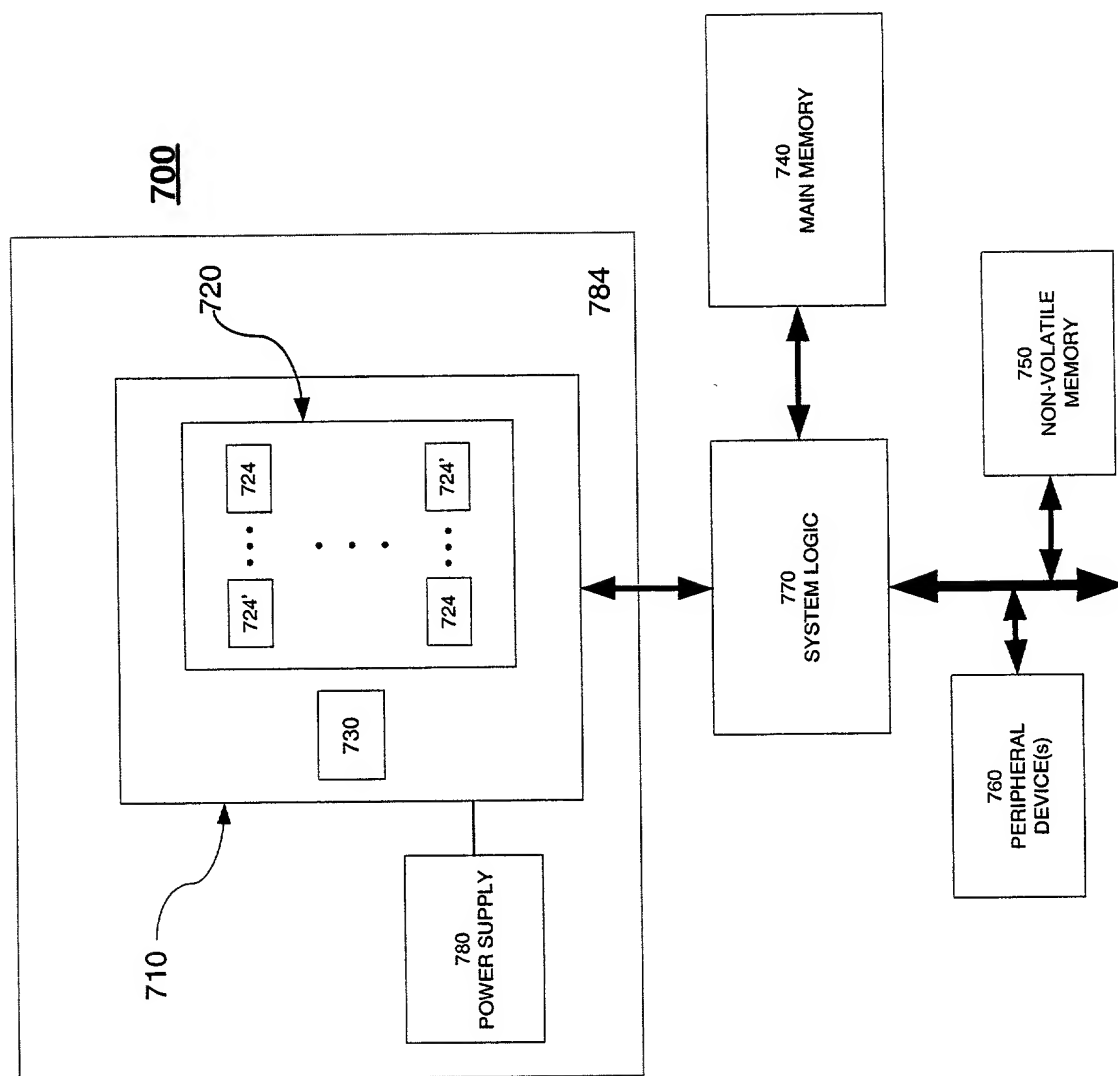


Fig. 7

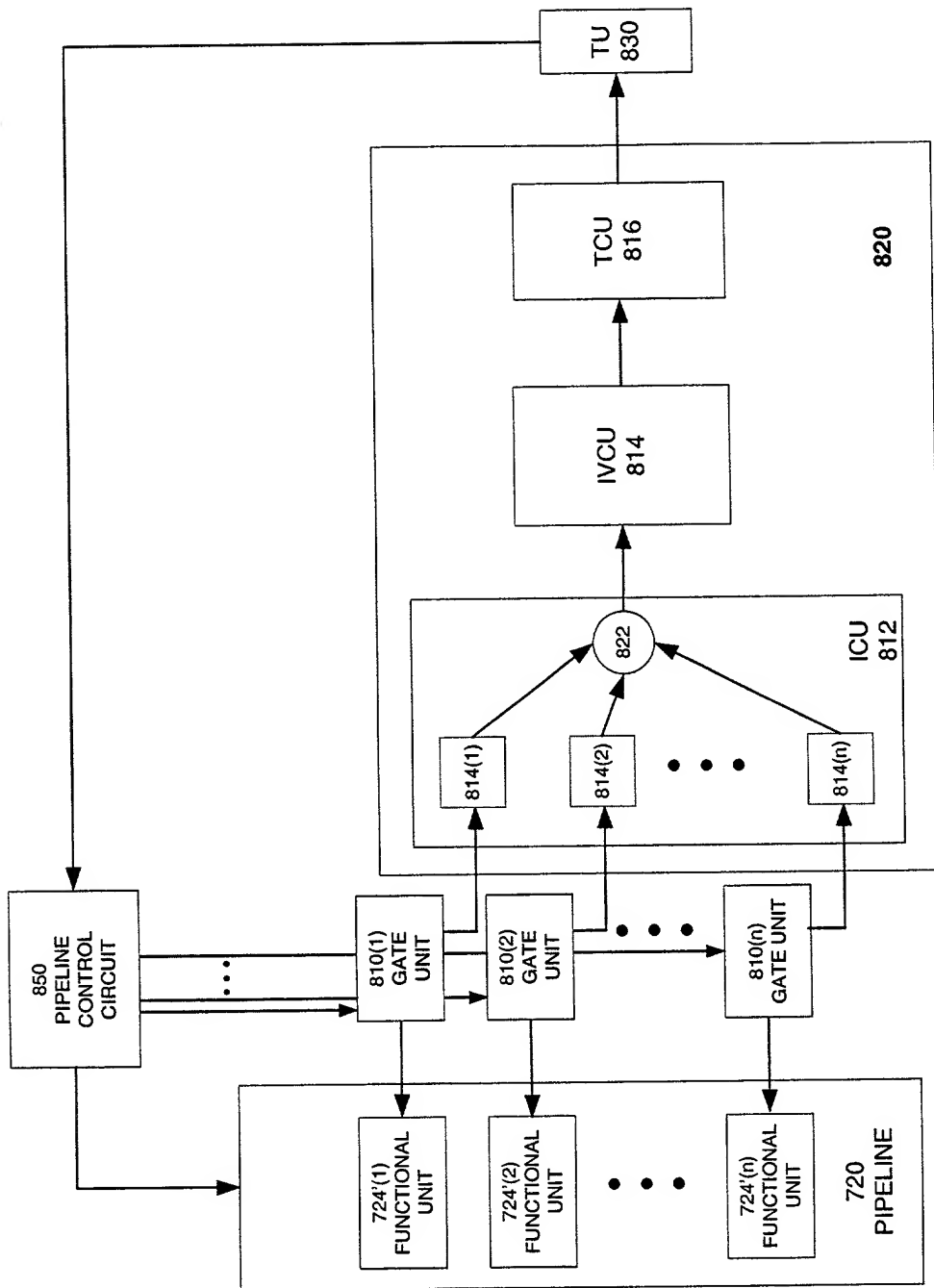


Fig. 8A



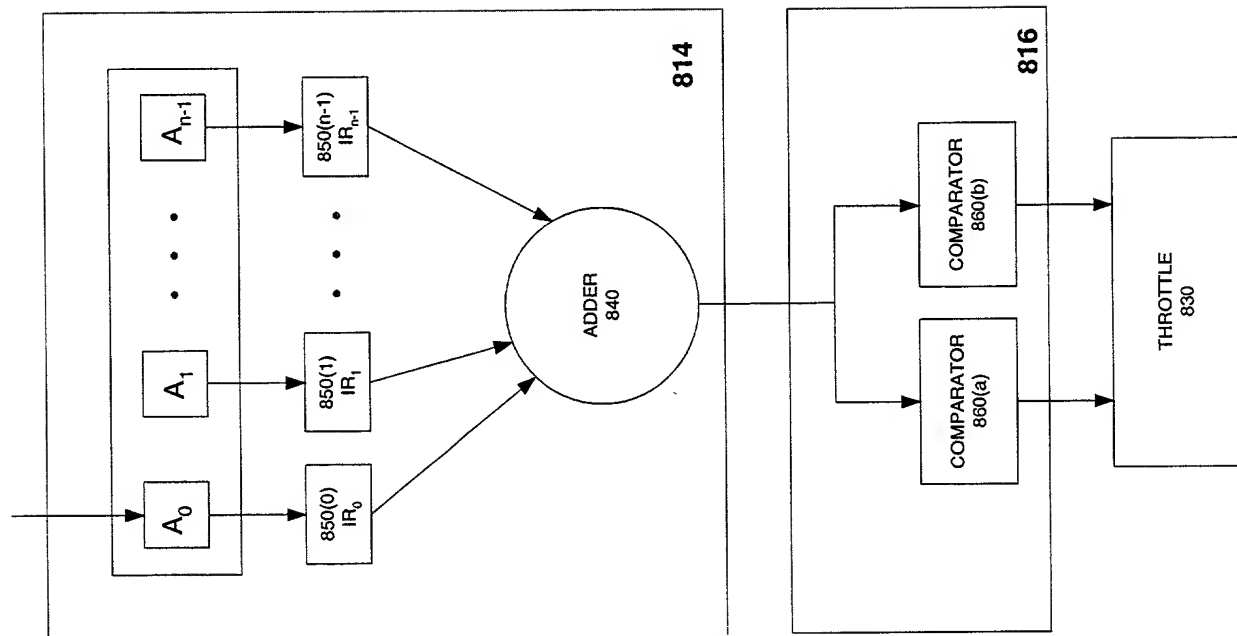


Fig. 8B

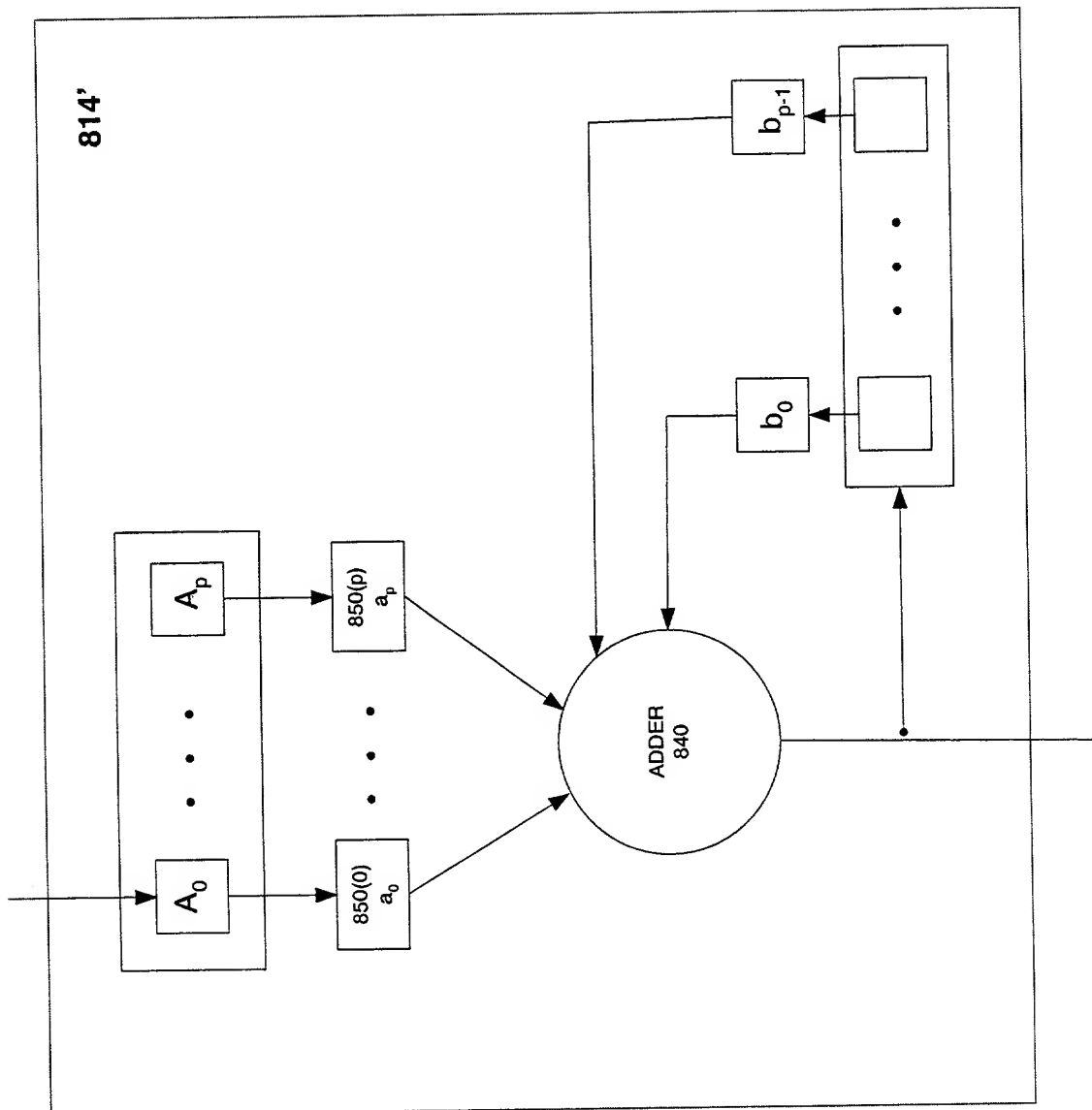


Fig. 8C

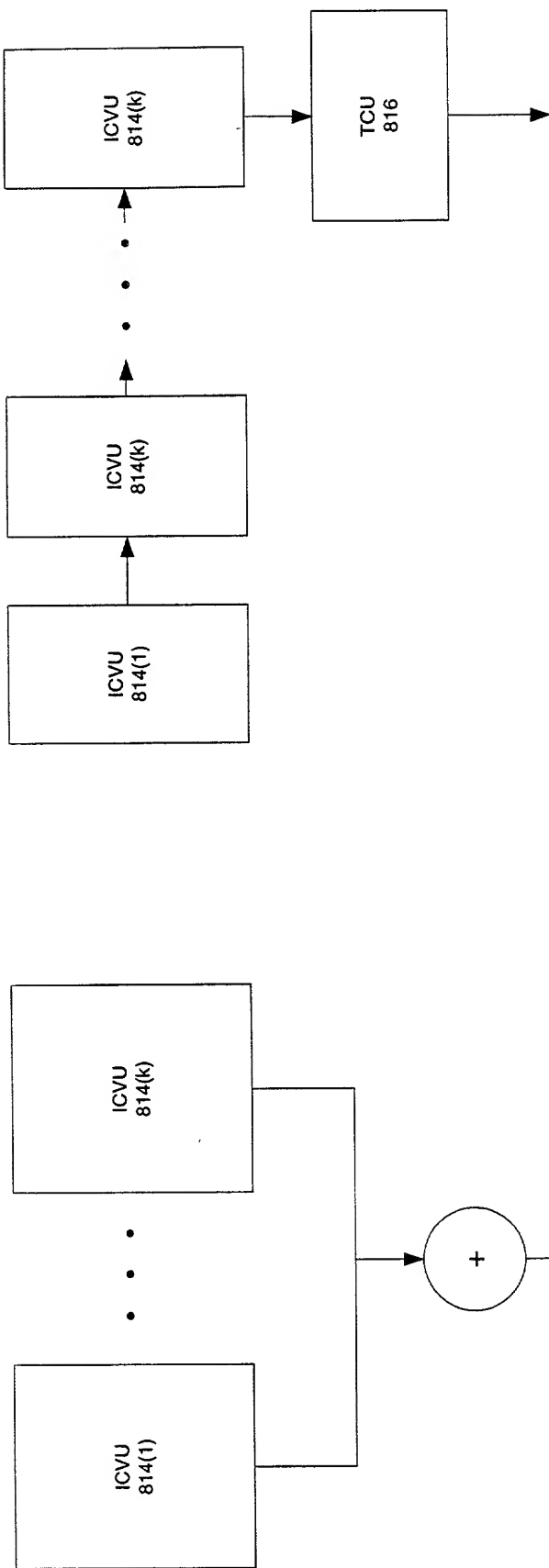


Fig. 8D

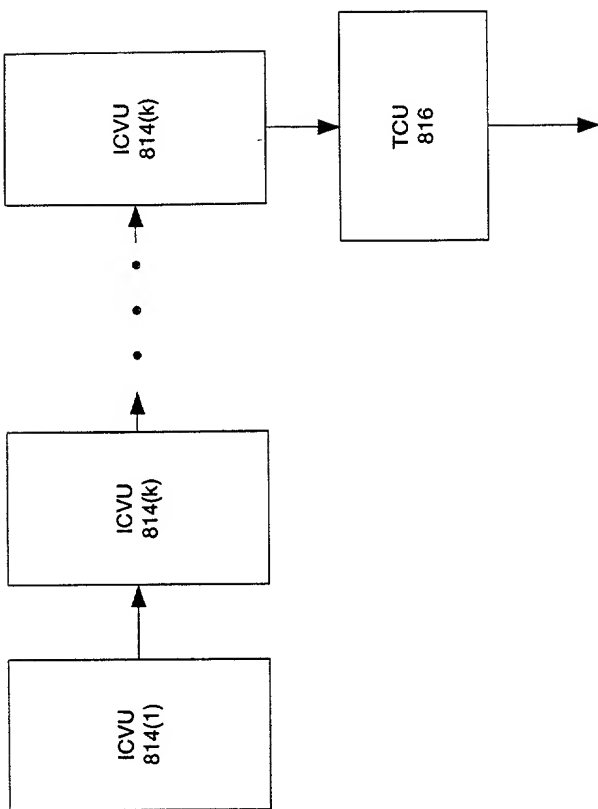


Fig. 8E

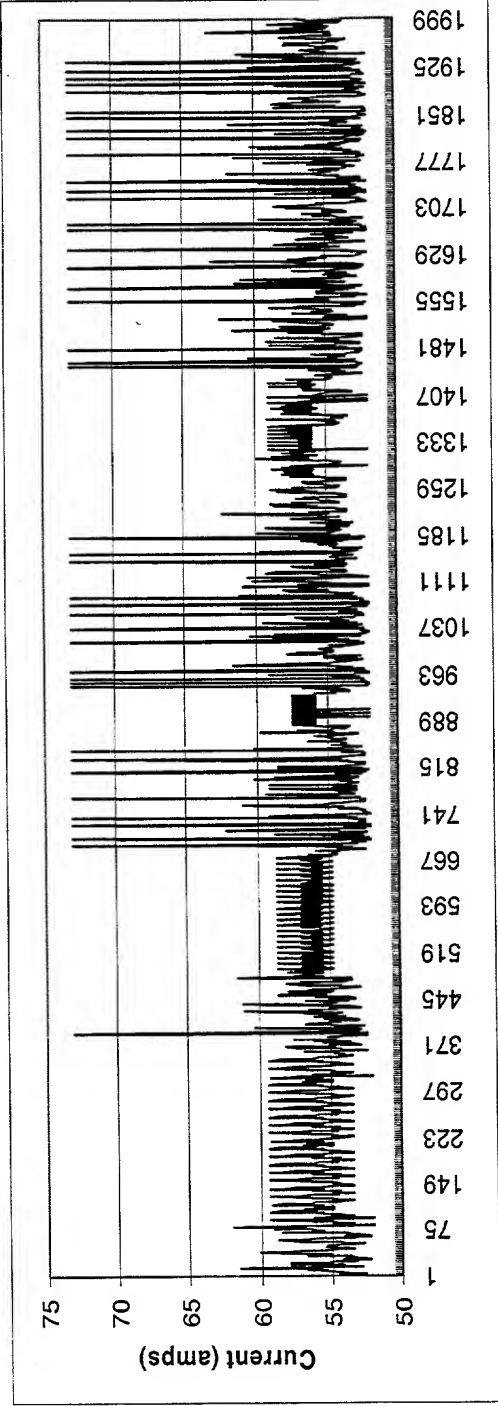


Fig. 9

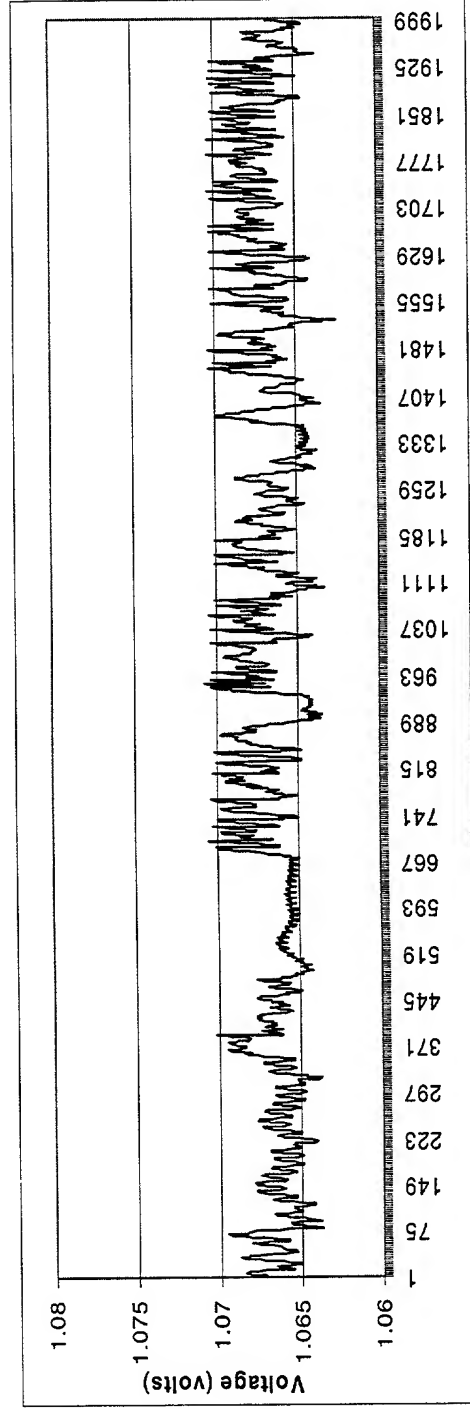


Fig. 10

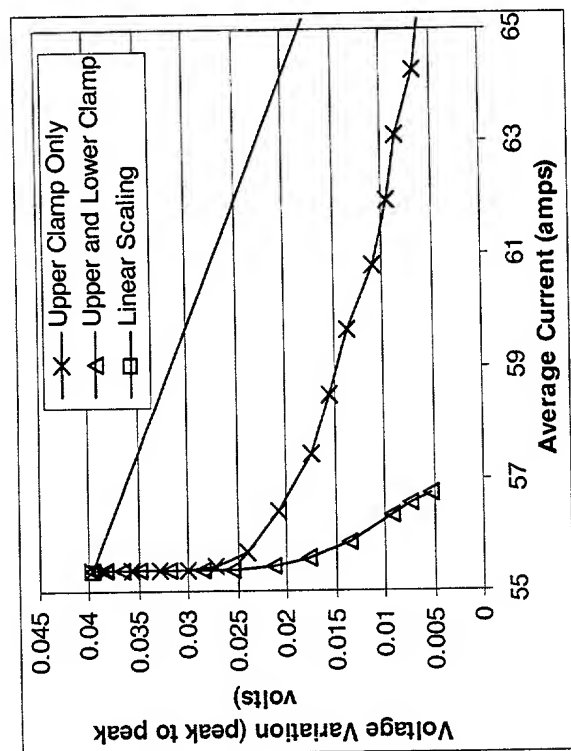


Fig. 11

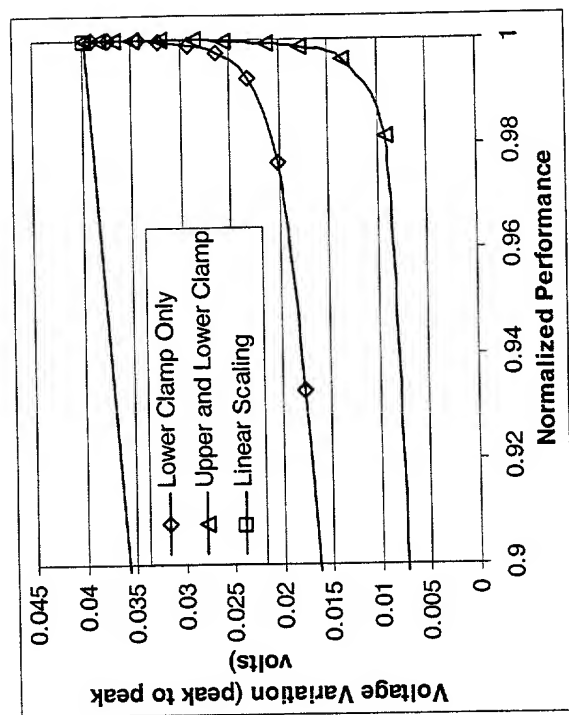


Fig. 12